Seek B1

Listing of Claims

Claim 1 (currently amended): An integrated circuit comprising:

a memory array having a first plane, a second plane, a third plane, and a fourth plane, wherein ~~the memory array is divided into~~ a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition ~~m partitions, wherein m is an integer greater than or equal to two~~; and

~~a microcontroller coupled to~~ a status register coupled to the memory array, wherein the status register ~~reports status information of m memory partitions~~ provides status information of the first plane, the second plane, the third plane, and the fourth plane.

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Claim 2 (currently amended): The integrated circuit of claim 1, wherein ~~the memory array is coupled to the status register by a decoder circuit~~ the first partition of the memory array comprises the second plane and the second partition of the memory array comprises the first plane, third plane, and the fourth plane.

Claim 3 (currently amended): The integrated circuit of claim 1, further comprising:

~~the~~ a microcontroller coupled to ~~a logic block;~~ the status register, wherein the microcontroller supplies control signals to the status register.

~~the logic block coupled to the status register;~~

~~the status register coupled to a user interface.~~

Claim 4 (currently amended): The integrated circuit of claim 1, wherein the first plane, the second plane, the third plane, and the fourth plane comprise equal memory storage capacities. ~~further comprising:~~

~~the user interface coupled to an address latch;~~

~~the address latch coupled to the logic block.~~

Claim 5 (currently amended): The integrated circuit of claim 3, further comprising:

~~wherein the~~ an user interface coupled to the status register, wherein the user interface communicates status register information to be used to decide subsequent operations.

Claim 6 (currently amended): A method of reading while writing to a memory array, comprising:

dividing the memory array into n planes, wherein n is an integer greater than ~~or equal to~~ two;

defining a write partition, wherein the write partition is a single plane of the memory array;

defining a read partition, wherein the read partition is made up of all of the remaining n planes of the memory array; and

providing the status of the read partition and the write partition of the memory array with a single status register.

Claim 7 (original): The method of claim 6, wherein the memory array consists of multiple 4 Mb memory planes.

Claim 8 (original): The method of claim 7, wherein the multiple 4 Mb memory planes consist of nonvolatile memory cells.

Claim 9 (original): The method of claim 8, wherein the nonvolatile memory cell is a flash memory cell.

Claim 10 (original): The method of claim 7, wherein the write partition has a dynamic memory address, wherein the memory address changes any time a program or erase operation begins or resumes in a new memory plane.

Claim 11 (original): The method of claim 7, wherein if no program or erase operation is performed, the read partition and the write partition are allocated to the same memory location.

Claims 12-17 (canceled)

Claim 18 (currently amended): An apparatus comprising:

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means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time; and

means for monitoring the operations performed on the memory array.

Claim 19 (original): The apparatus of claim 18 further comprising a means for communicating the status of the operations performed on the memory array to a user.